

523,385

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
19 February 2004 (19.02.2004)

PCT

(10) International Publication Number  
**WO 2004/015692 A2**

(51) International Patent Classification<sup>7</sup>: **G11B 7/00**

(21) International Application Number:  
PCT/IB2003/003293

(22) International Filing Date: 21 July 2003 (21.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
02078239.7 6 August 2002 (06.08.2002) EP

(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **VOORMAN, Johannes, O.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **DE JONG, Gerben, W.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **BREKELMANS, Johannes, H., A.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: **DUIJVESTIJN, Adrianus, J.**; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

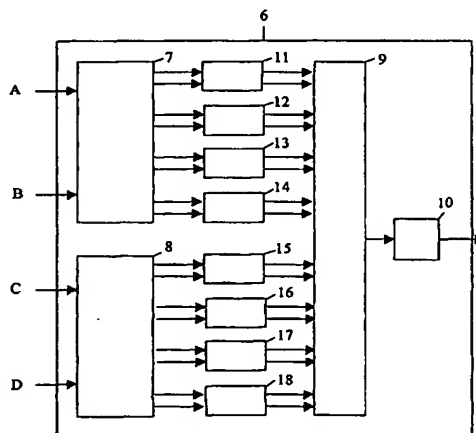
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

**Declaration under Rule 4.17:**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO

[Continued on next page]

(54) Title: OPTICAL DISK SYSTEM WITH DELAYLINELESS DELAY-DIFFERENCE DETECTOR



(57) **Abstract:** Optical disk systems comprising photo detectors (1) for detecting optical disks comprising amplifiers and slicers (2-5) and delay-difference detectors (6) for detecting delay differences in sliced amplified detection signals are improved by installing delaylineless delay-difference detectors (6) comprising combinatorial-logic circuits (7,8) like inverters, ORs, NORs, ANDs, NANDs and sequential-logic circuits (11-18) like SetResetFlipFlops. Without the prior art delay lines, said delay-difference detectors (6) are of a lower complexity and low costly and can be well integrated. By introducing a first pair of sequential-logic circuits (11,12,15,16) for detecting delay differences between rising edges and a second pair of sequential-logic circuits (13,14,17,18) for detecting delay differences between falling edges, both kinds of edges are being used and the influence of time-jitter is less compared to the situation where just one kind of edge is used. Said delay-difference detector (6) further comprises an analog adder/subtractor (9) for adding/subtracting sequential-logic circuit output signals and low pass filter(s) (10) located before or after said adder/subtractor (9).



WO 2004/015692 A2